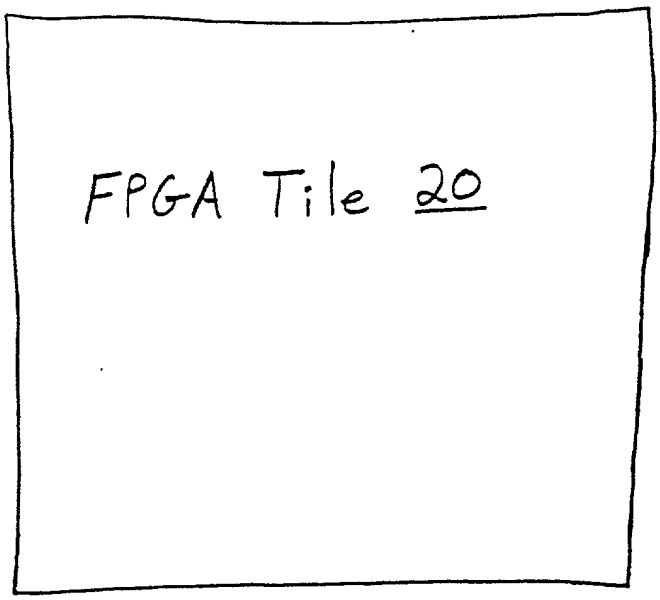


FIG. 1

1000659 050302

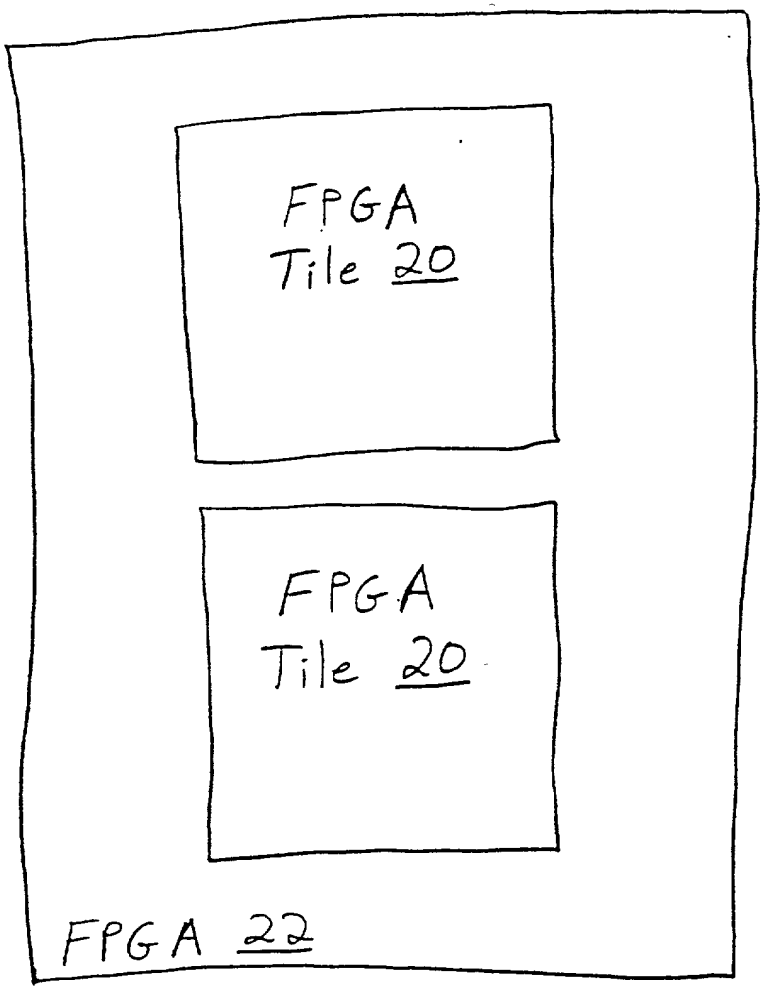


FIG. 2

4005535 v1 050305

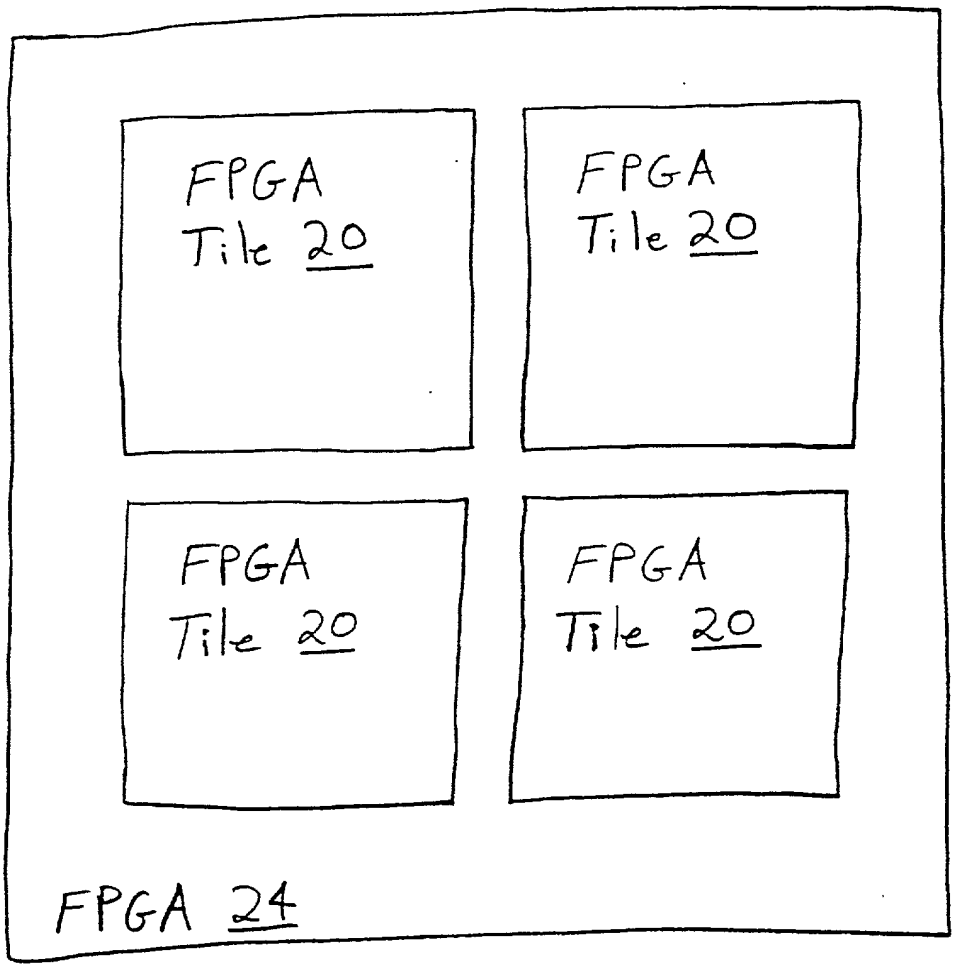


FIG. 3A

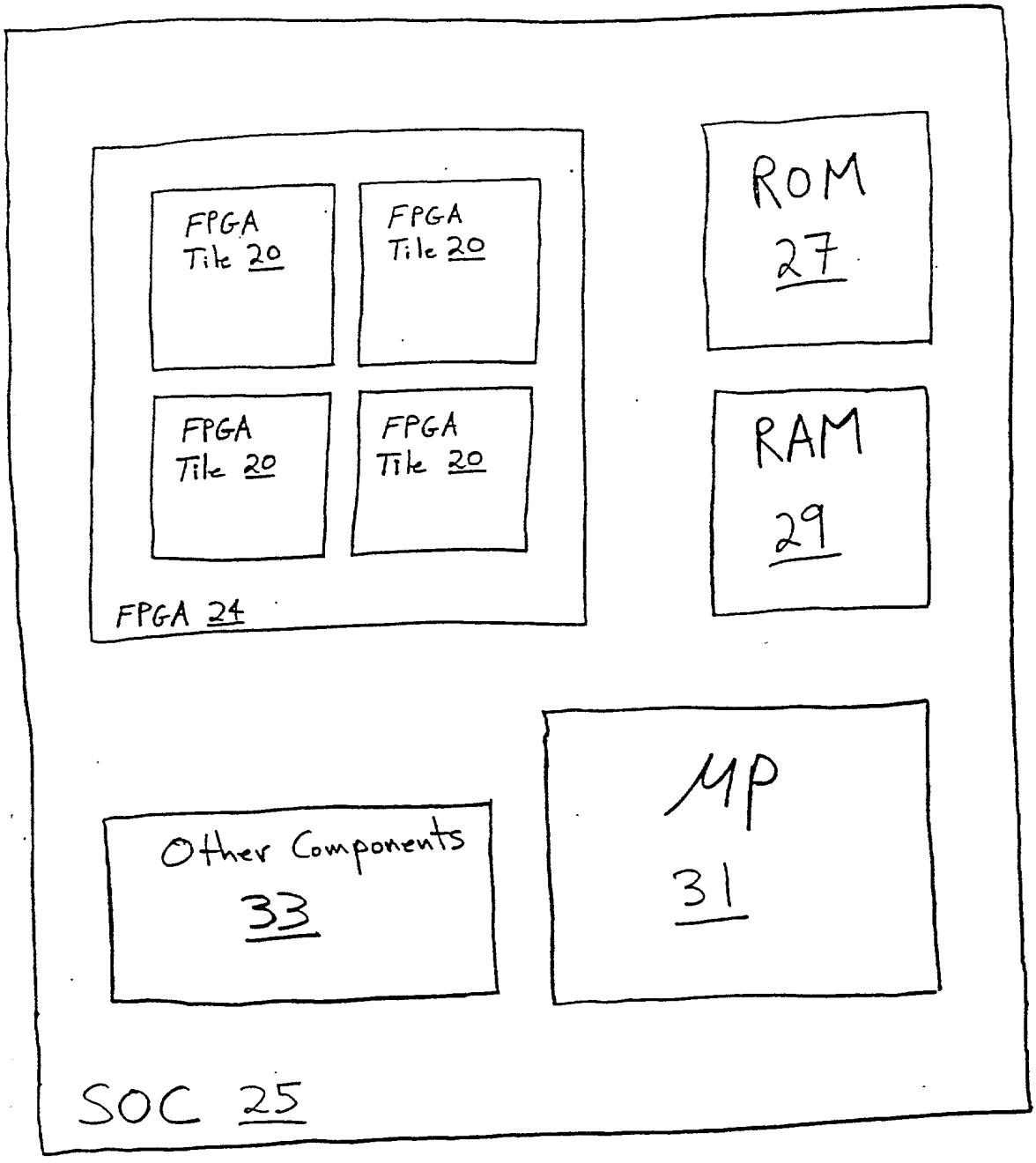

FPGA Tile 20
FPGA Tile 20
FPGA Tile 20
FPGA Tile 20
FPGA 24
ROM 27
RAM 29
Other Components 33
MP 31
SOC 25

FIG. 3B

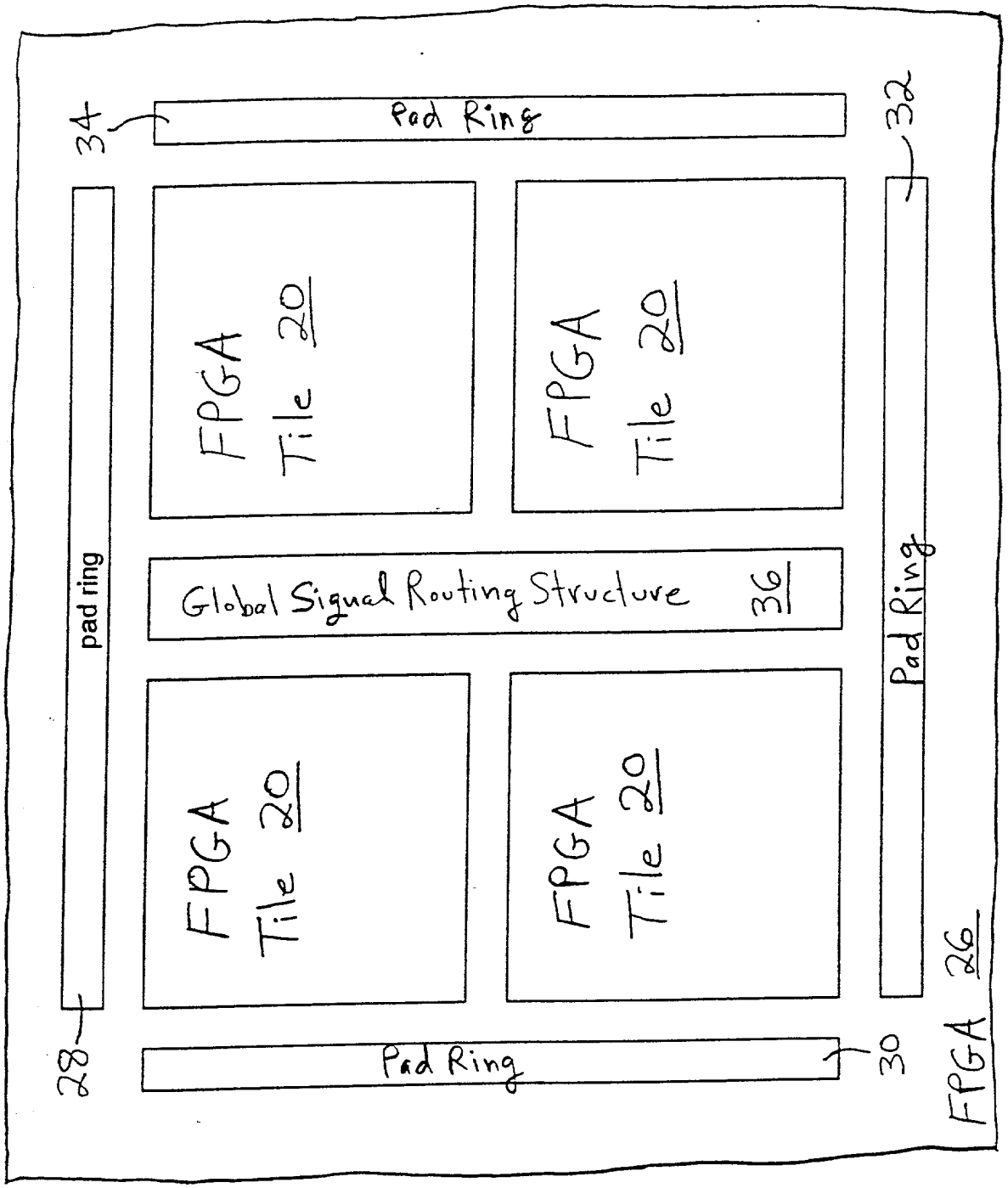

Pad Ring
34
32
pad ring
FPGA Tile 20
FPGA Tile 20
Global Signal Routing Structure 36
FPGA Tile 20
FPGA Tile 20
Pad Ring
28
Pad Ring
30
FPGA 26

FIG. 4

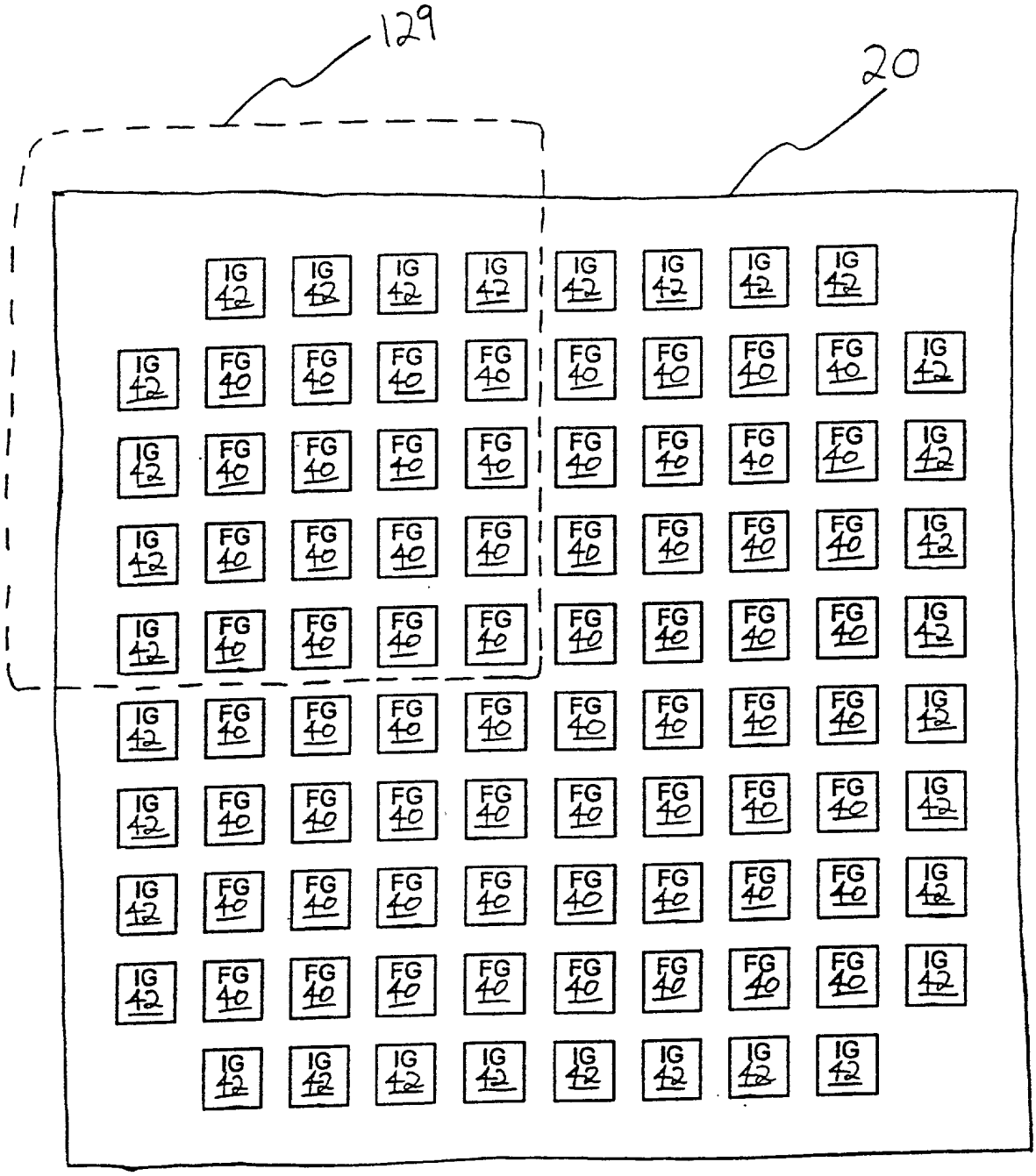


FIG. 5

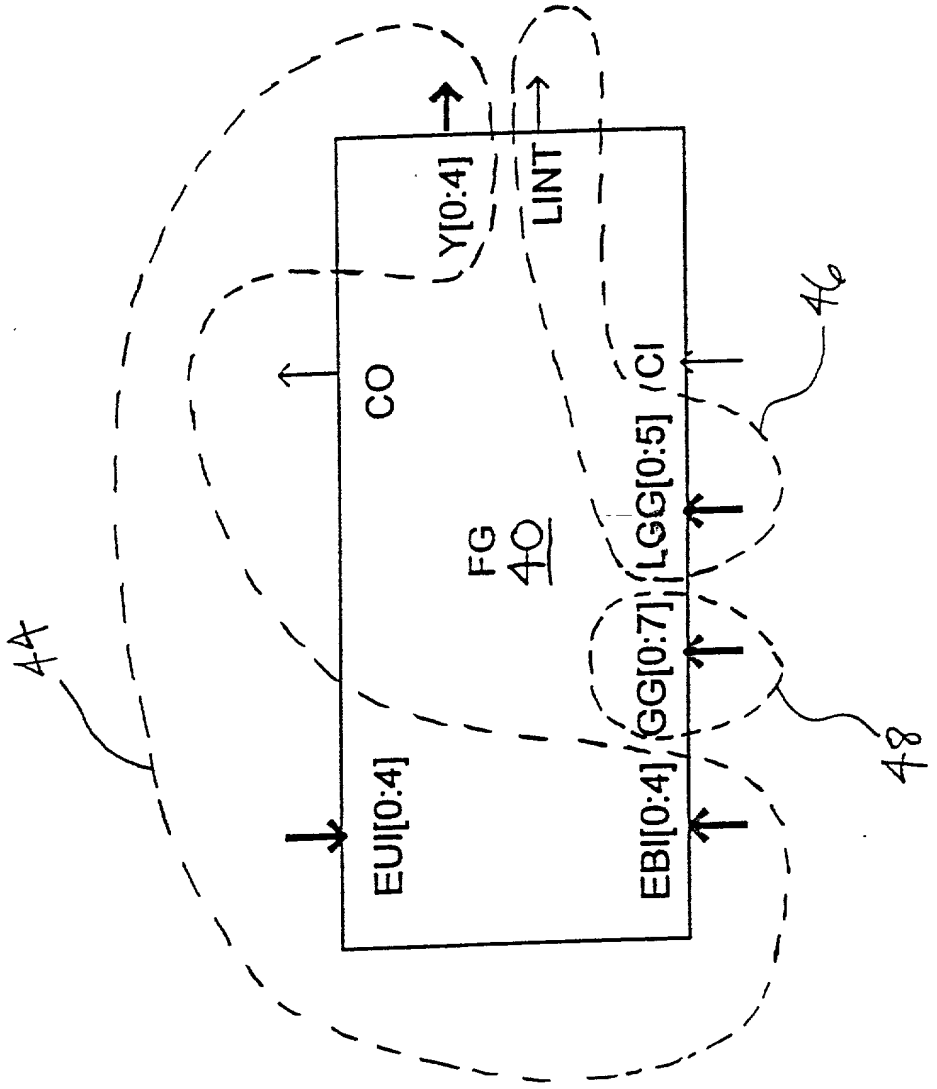


FIG. 6

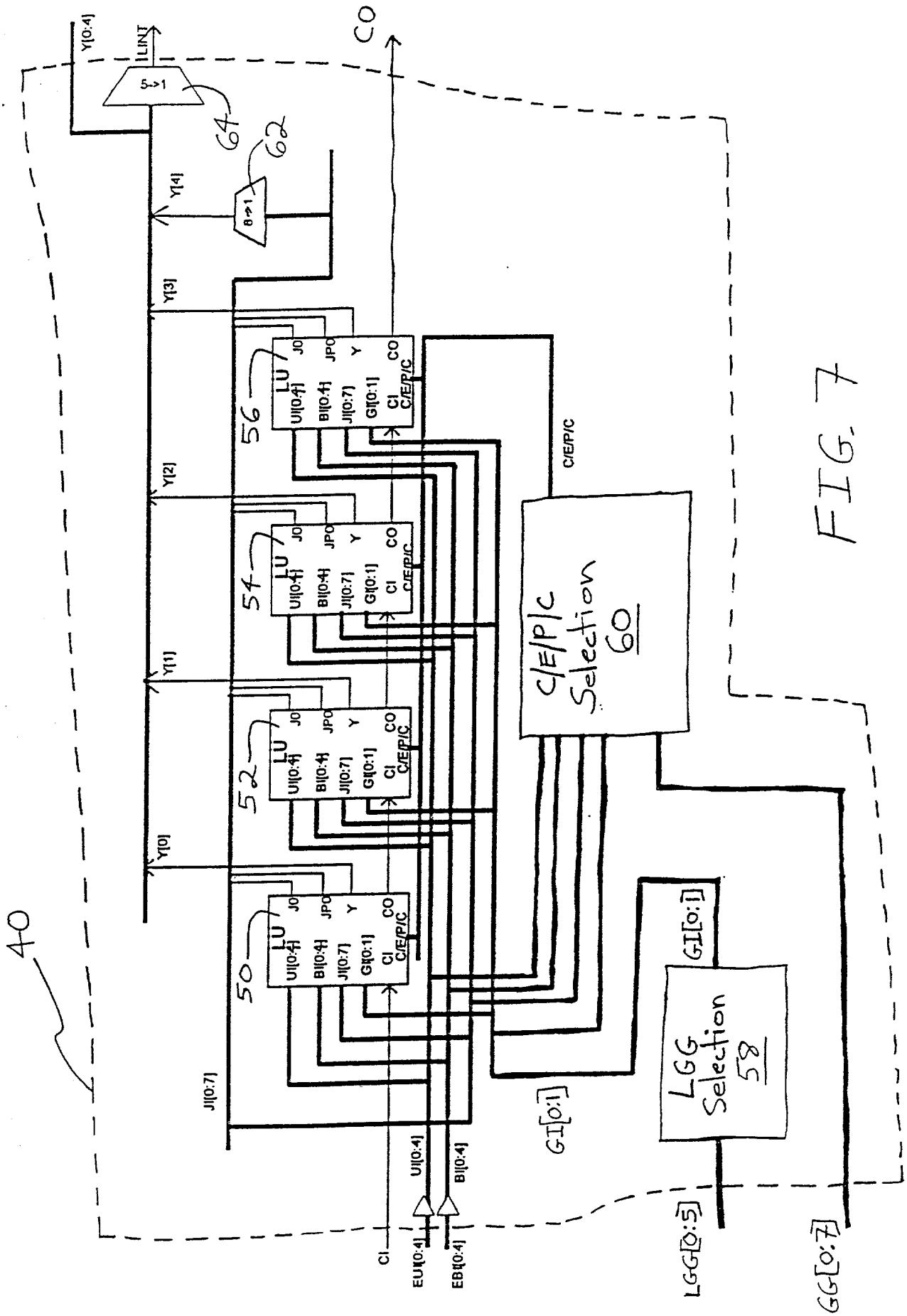

40
Y[0:4]
LINT
5->1
64
62
8->1
Y[4]
Y[3]
Y[2]
Y[1]
Y[0]
CO
LU
JO
JPO
Y
CO
UI[0:4]
BI[0:4]
JI[0:7]
GI[0:1]
CI
C/E/P/C
56
54
52
50
C/E/P/C
C/E/P/C Selection 60
GI[0:1]
LGG Selection 58
GI[0:1]
JI[0:7]
UI[0:4]
BI[0:4]
CI
EUI[0:4]
EBI[0:4]
LGG[0:5]
GG[0:7]

FIG. 7

ACT-317

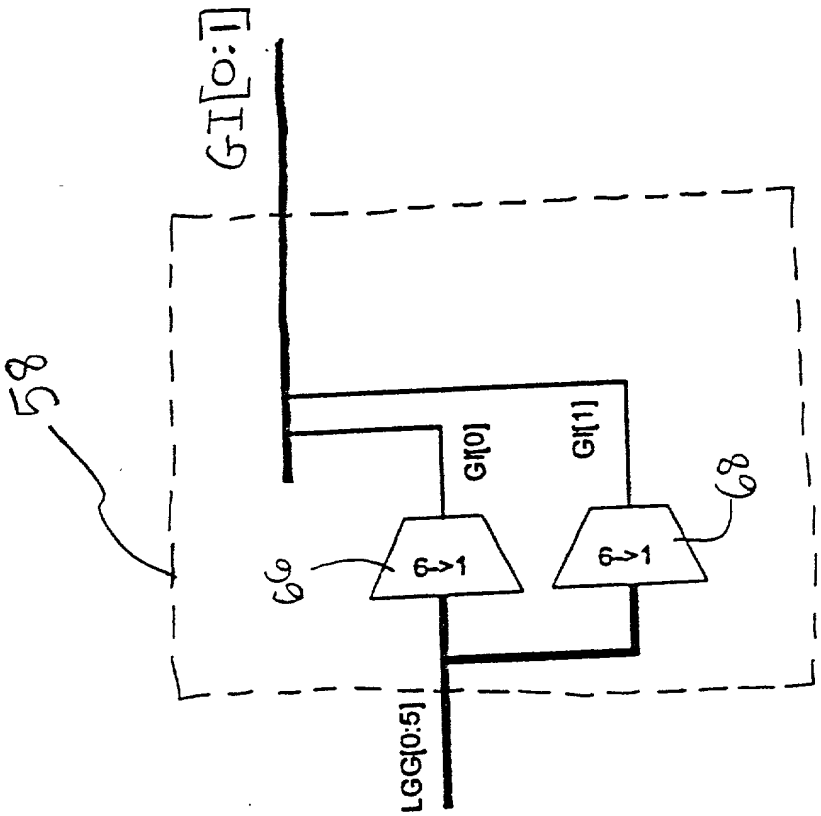


FIG. 8

EL 858979398 US

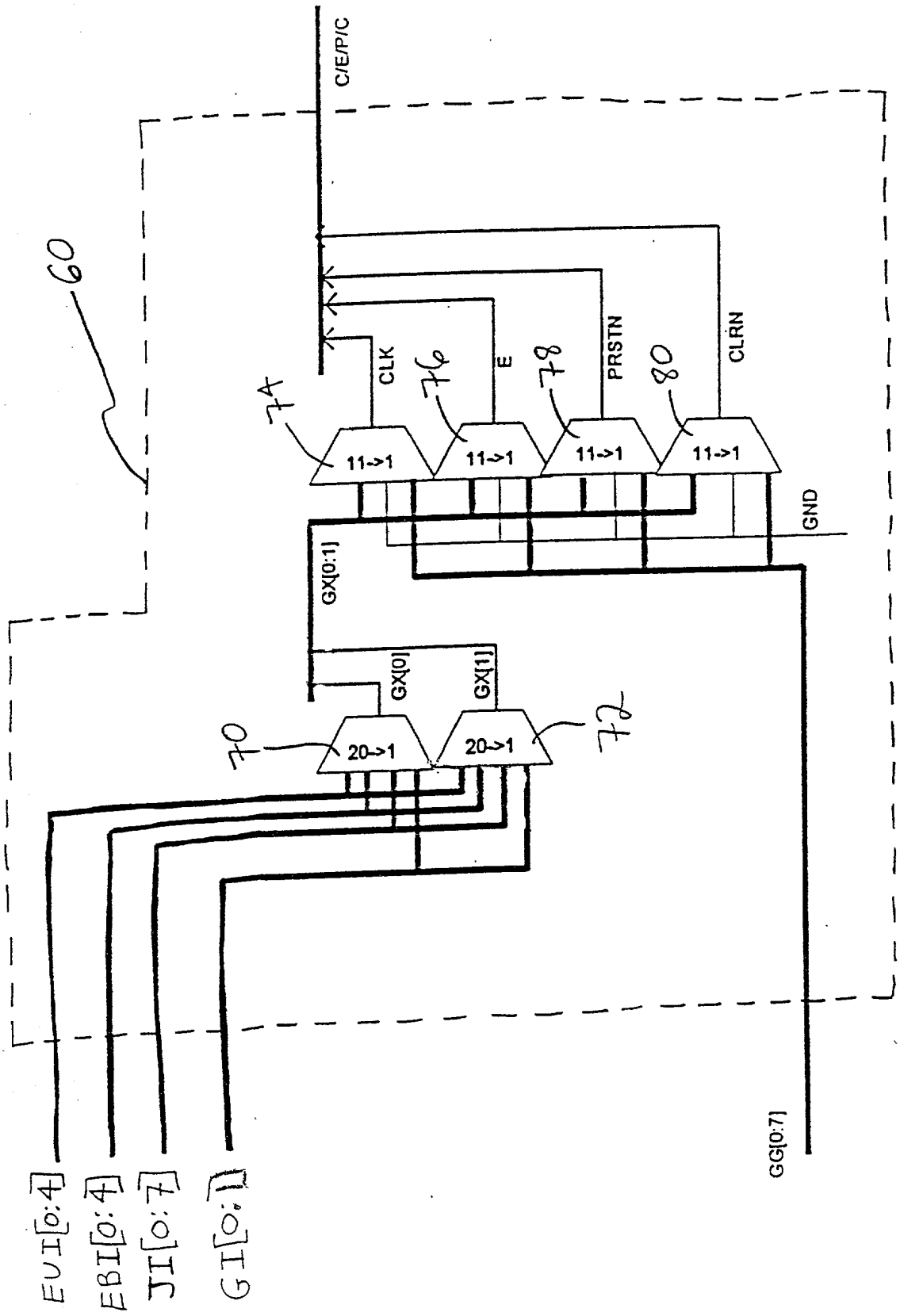

C/E/P/C
60
CLK
E
PRSTN
CLRN
74
76
78
80
11->1
11->1
11->1
11->1
GND
GX[0:1]
GX[0]
GX[1]
70
72
20->1
20->1
EUI[0:4]
EBI[0:4]
JI[0:7]
GI[0:1]
GG[0:7]

FIG. 9

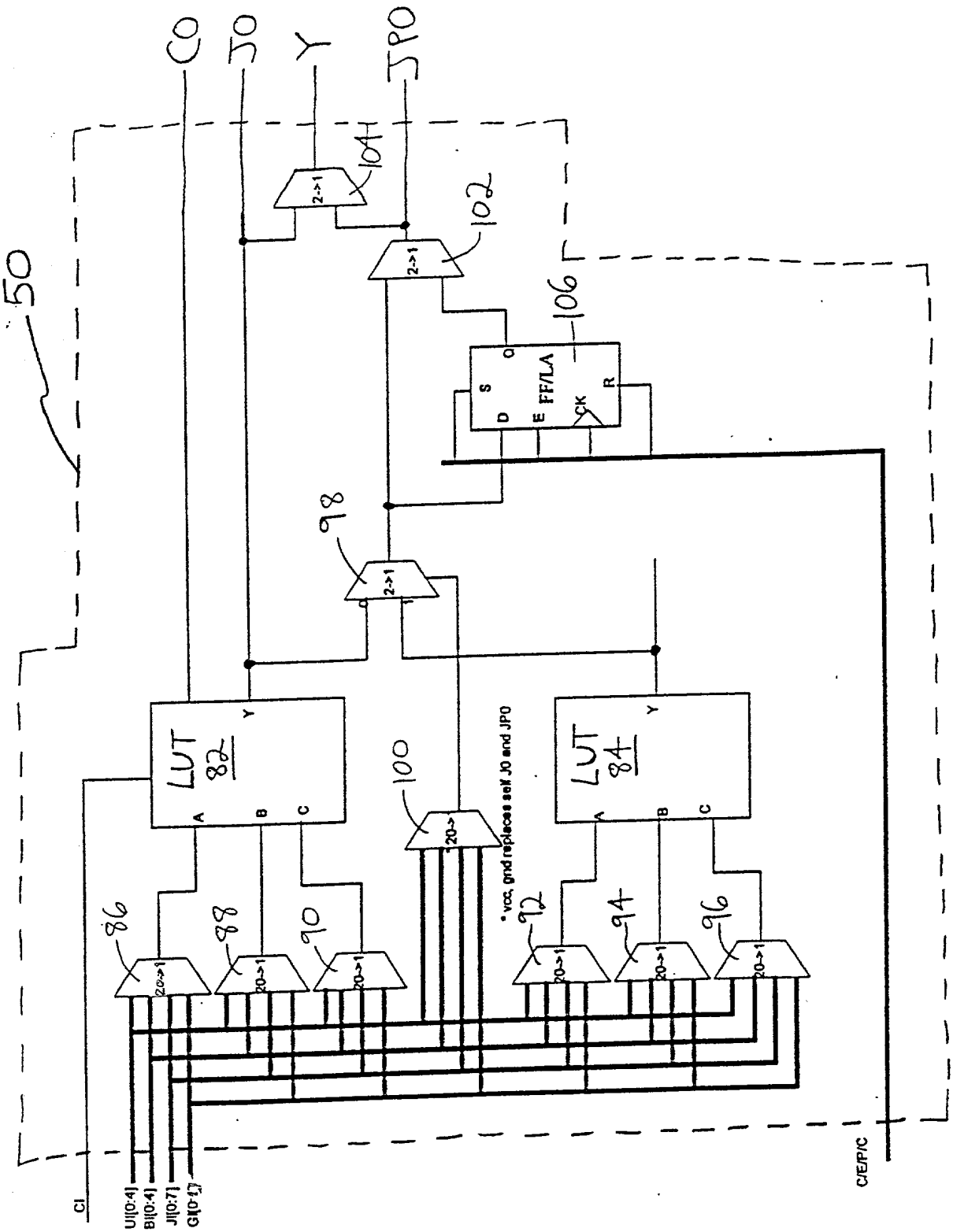

CO
JO
Y
JPO
50
104
102
106
2->1
FF/LA
D
E
S
CK
R
Q
98
LUT
82
84
A
B
C
Y
100
20->1
* vcc, gnd replaces self JO and JPO
86
88
90
92
94
96
CI
UI[0:4]
BI[0:4]
JI[0:7]
GI[0:7]
C/E/P/C

FIG. 10

ACT-317

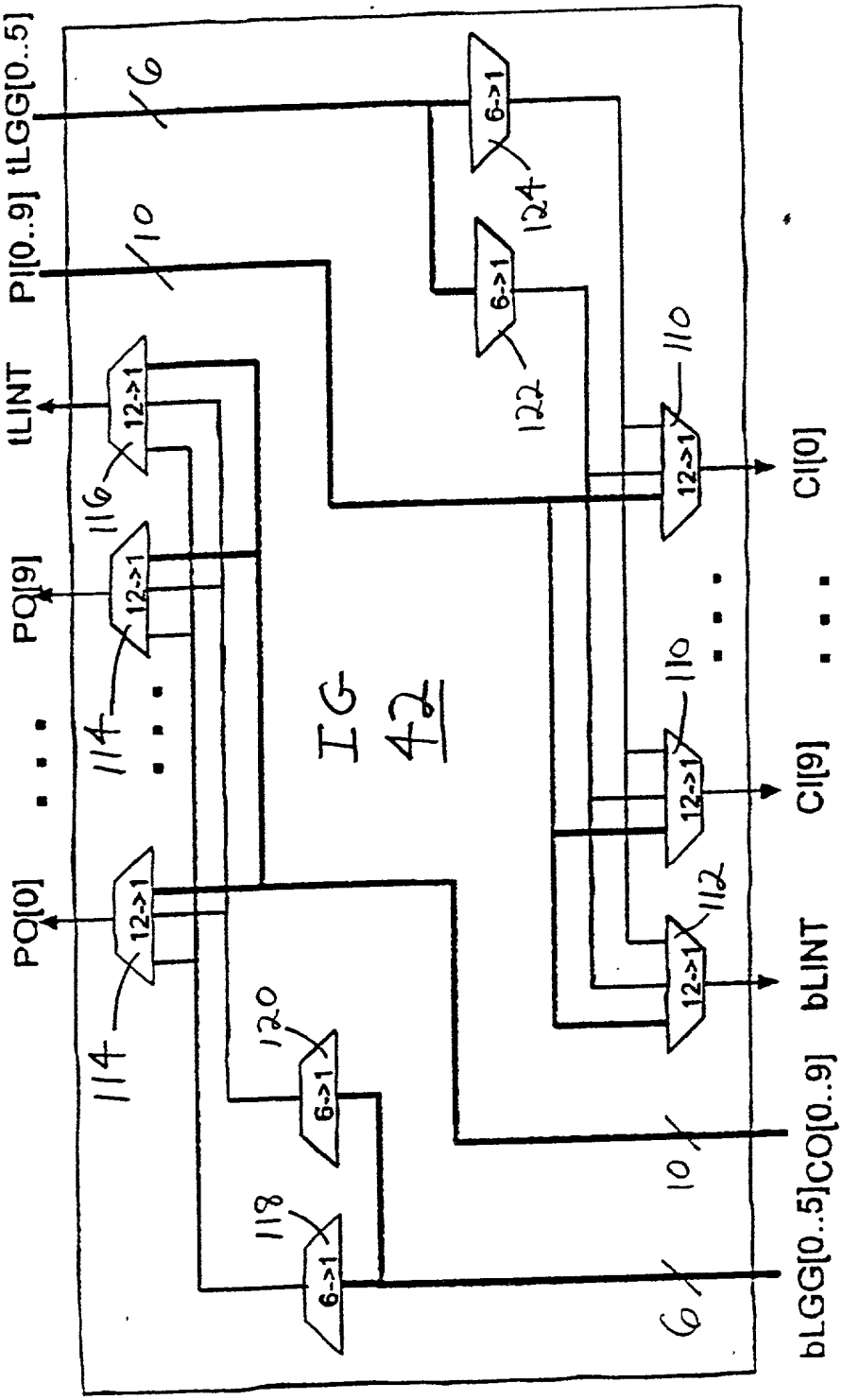


FIG. 11

Act-3:7

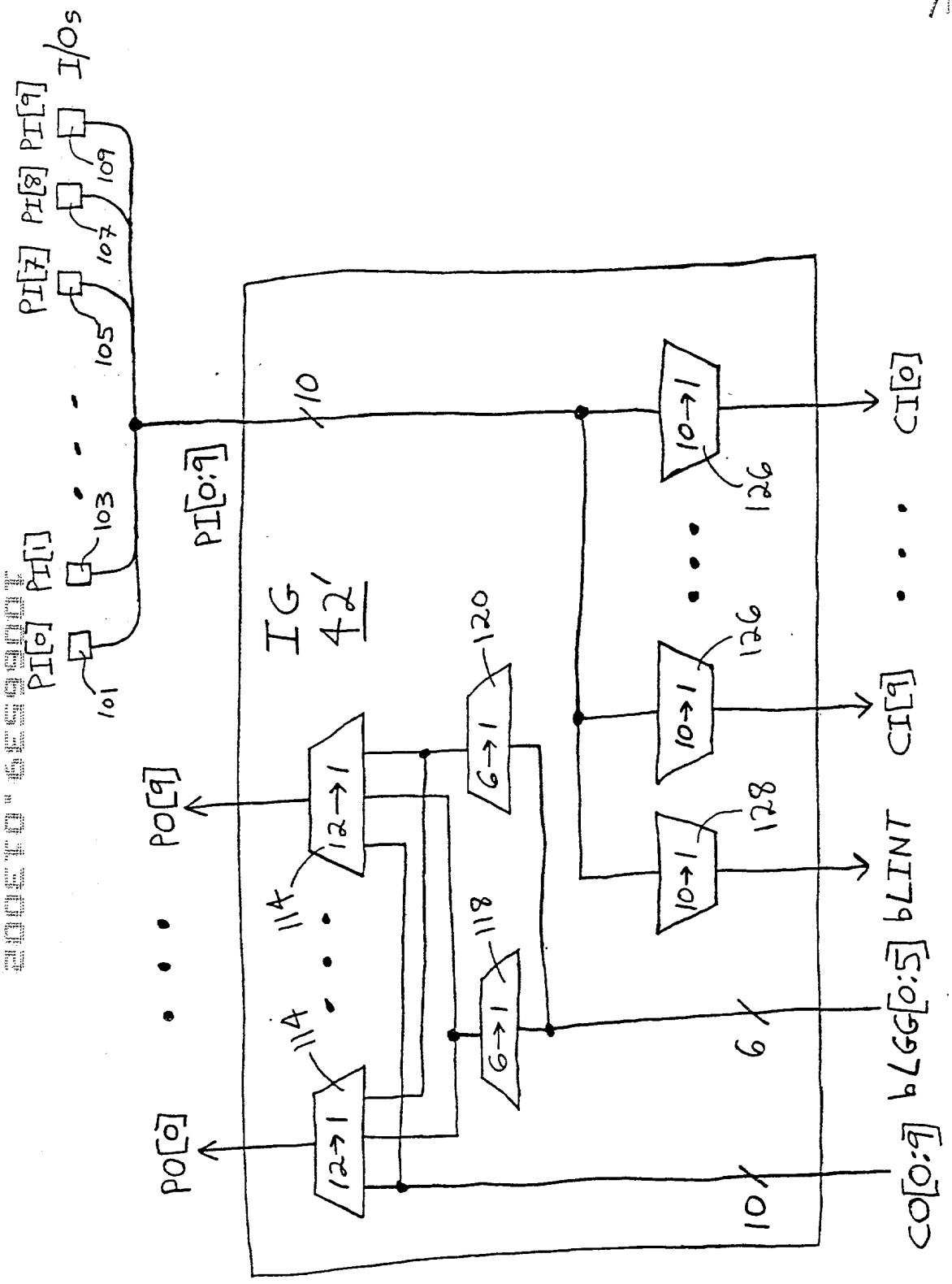

I/Os
PI[9]
PI[8]
PI[7]
PI[1]
PI[0]
109
107
105
103
101
PI[0:9]
110
IG
42'
12→1
6→1
10→1
114
118
120
126
128
PO[9]
PO[0]
CI[9]
CI[0]
9
10
bLINT
bLG[0:5]
CO[0:9]

FIG. 12

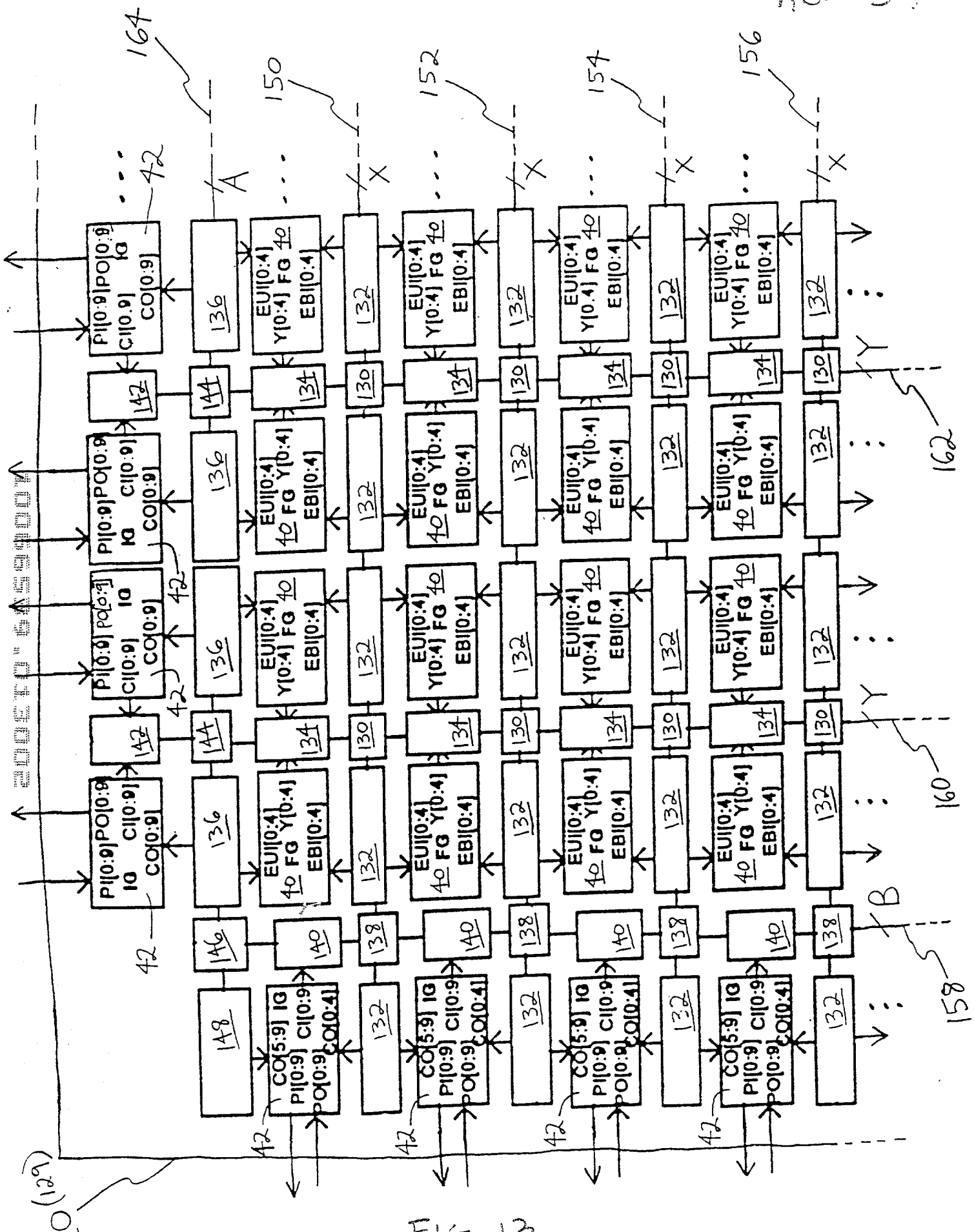

164
150
152
154
156
A
X
Y
B
160
162
158
20
129
42
132
130
134
136
138
140
142
144
146
148
PI[0:9] PO[0:9] IG CI[0:9] CO[0:9]
EUI[0:4] Y[0:4] FG EBI[0:4]
CO[5:9] IG PI[0:9] PO[0:9] CI[0:9] CO[0:4]

FIG. 13

ACT-317

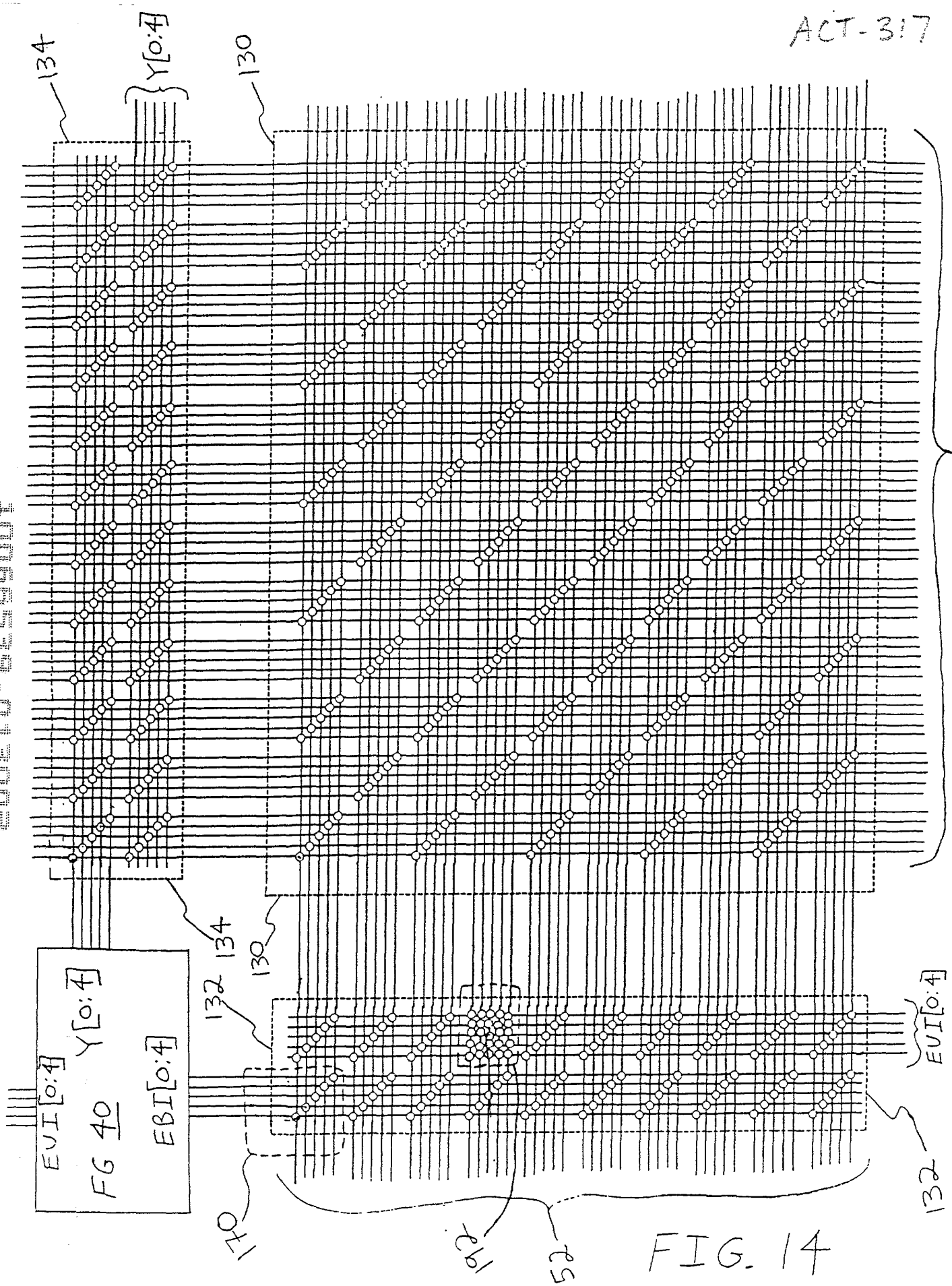


FIG. 14

ACT-317

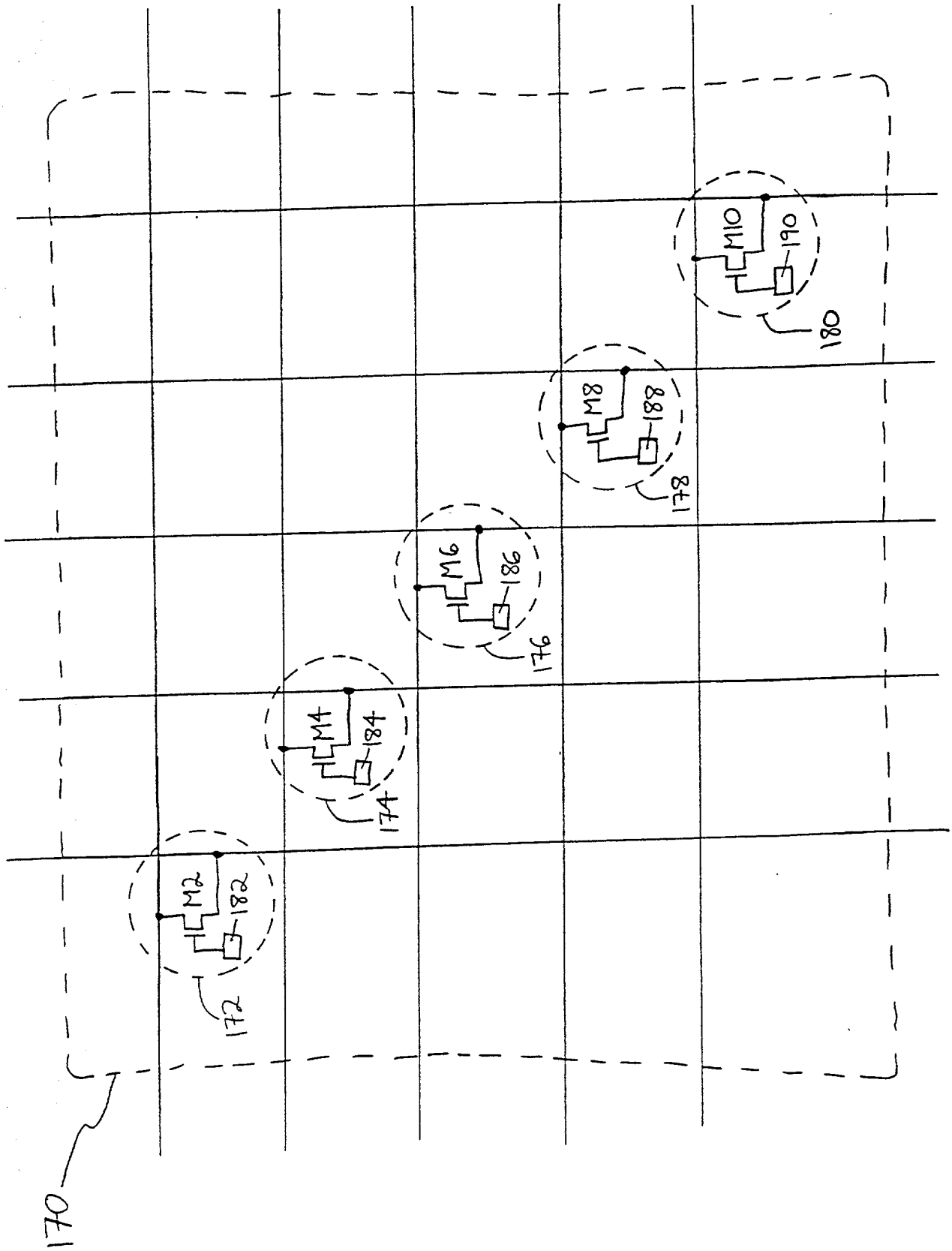


FIG. 15

ACT-317

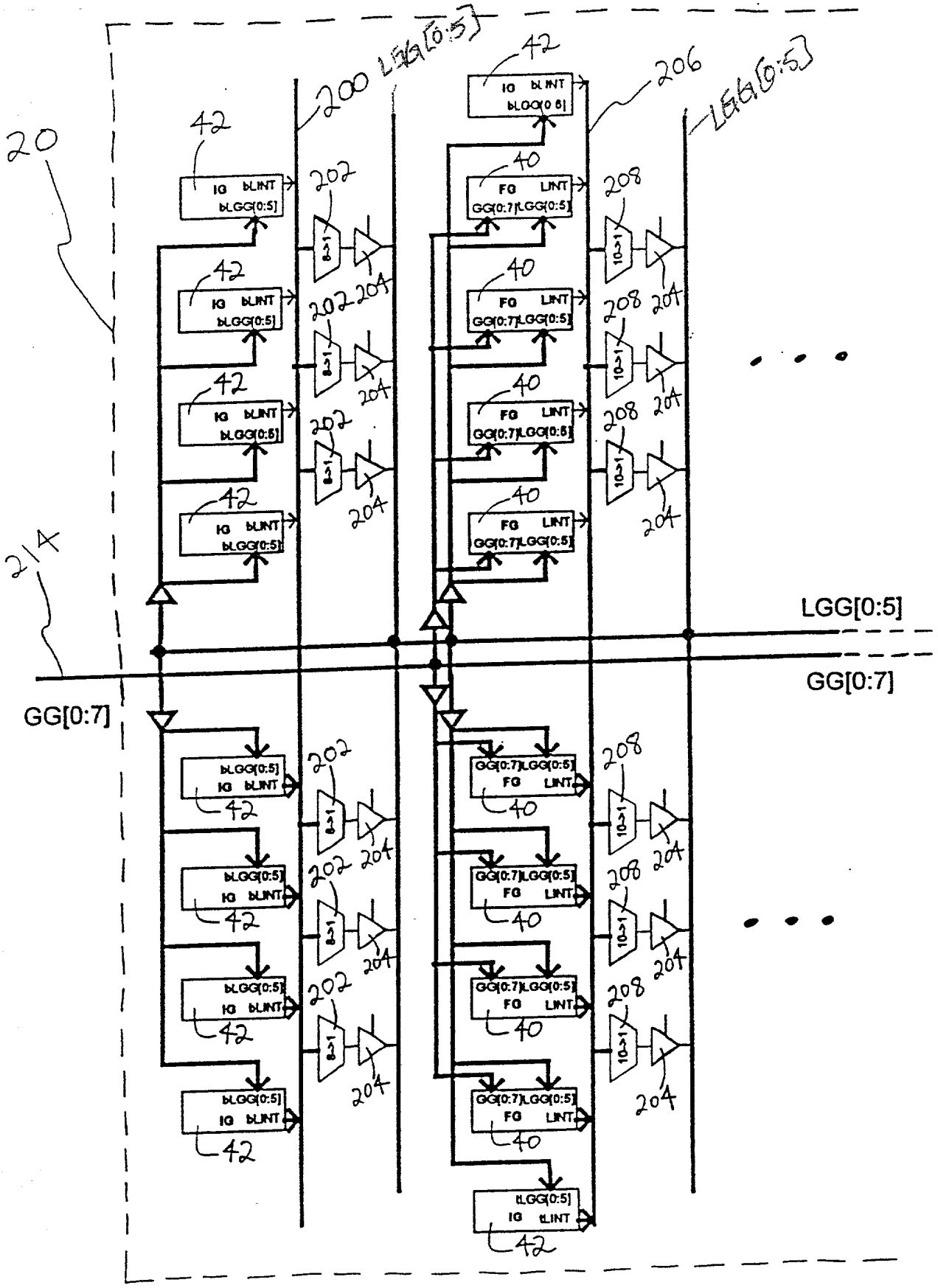


FIG. 16A

ACT. 3/7

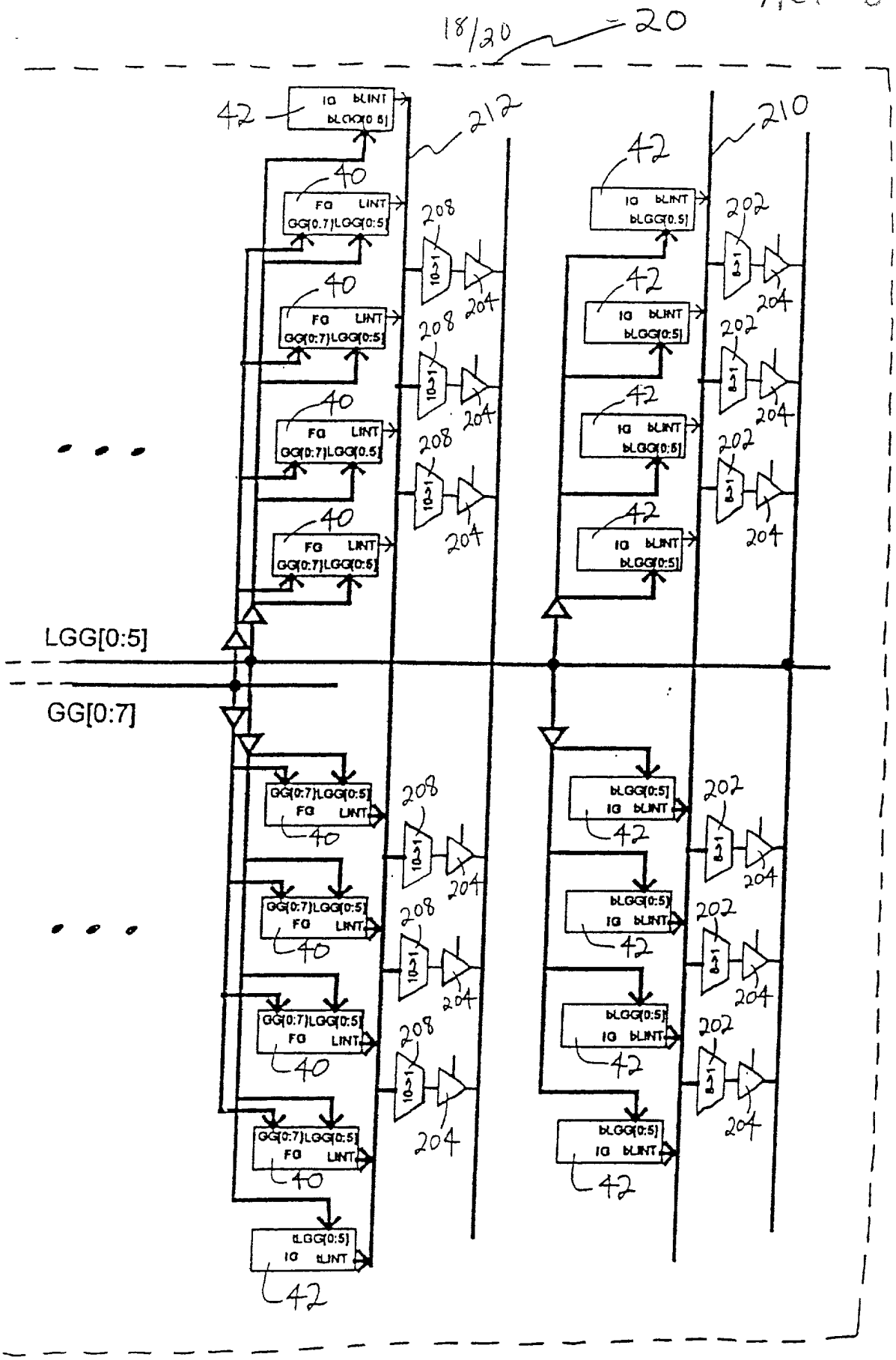


FIG. 16B

ACT-317

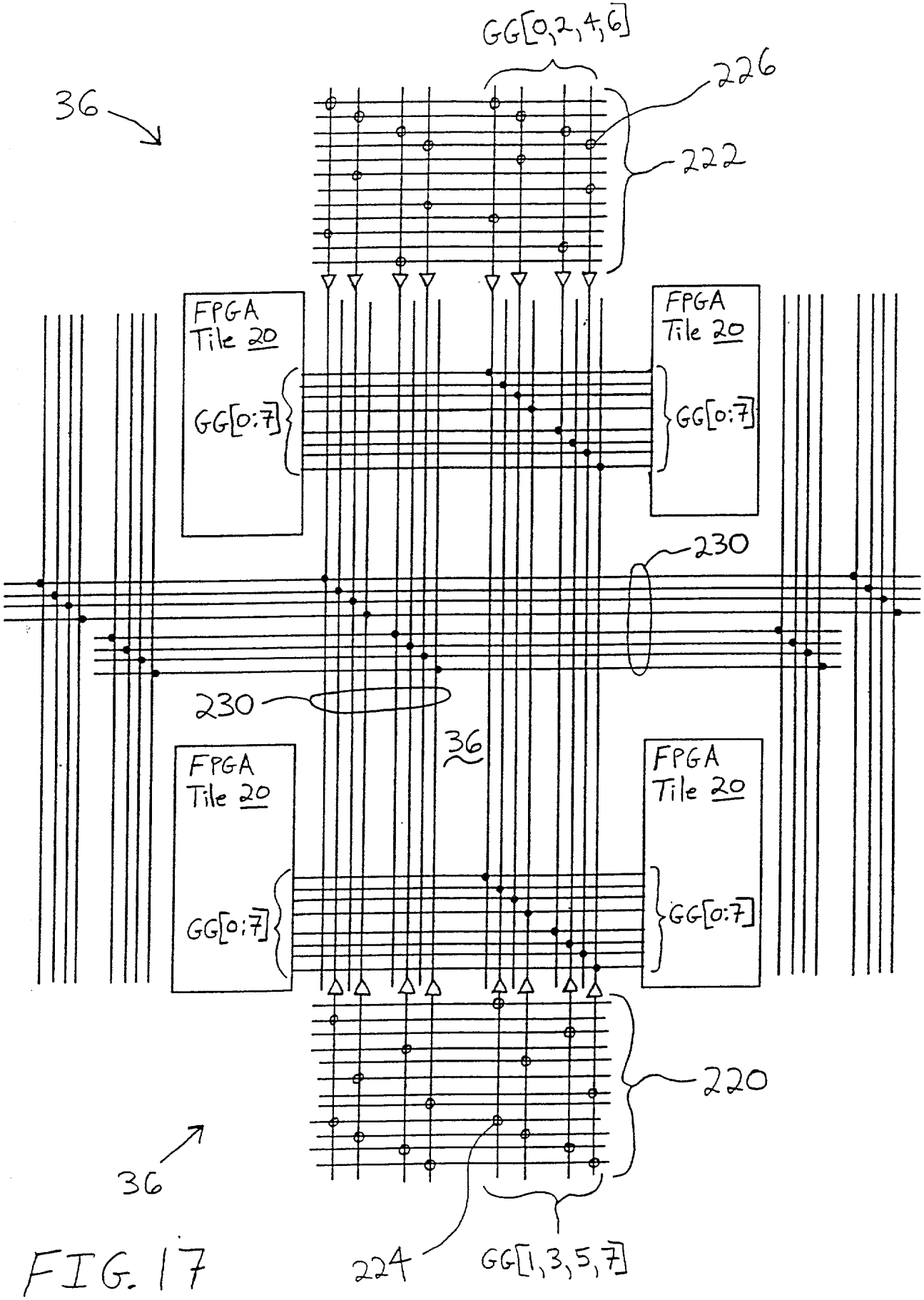


FIG. 17

Adobe Systems Incorporated

ACT-317

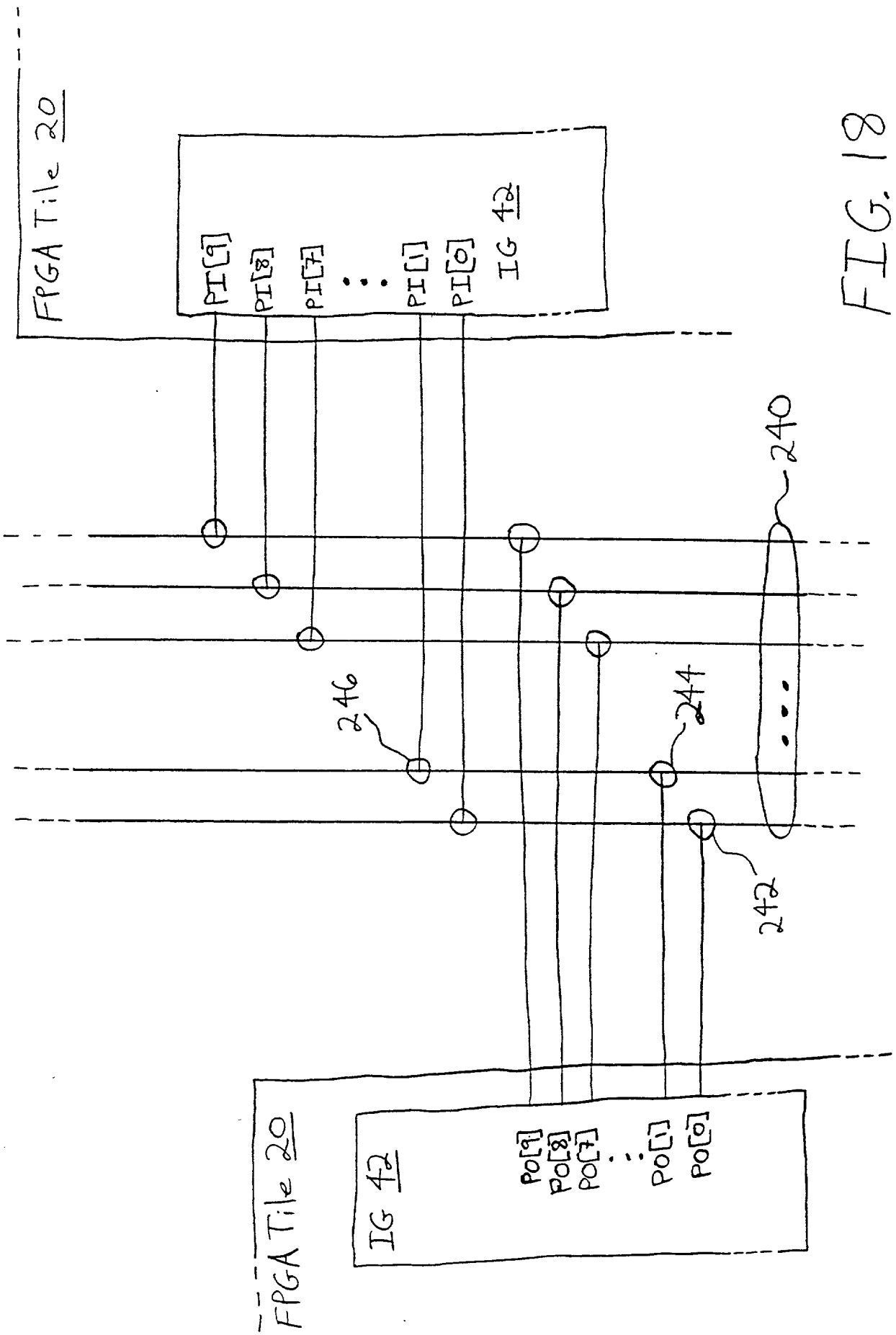


FIG. 18

D0C3E5 5E 0E3E0E

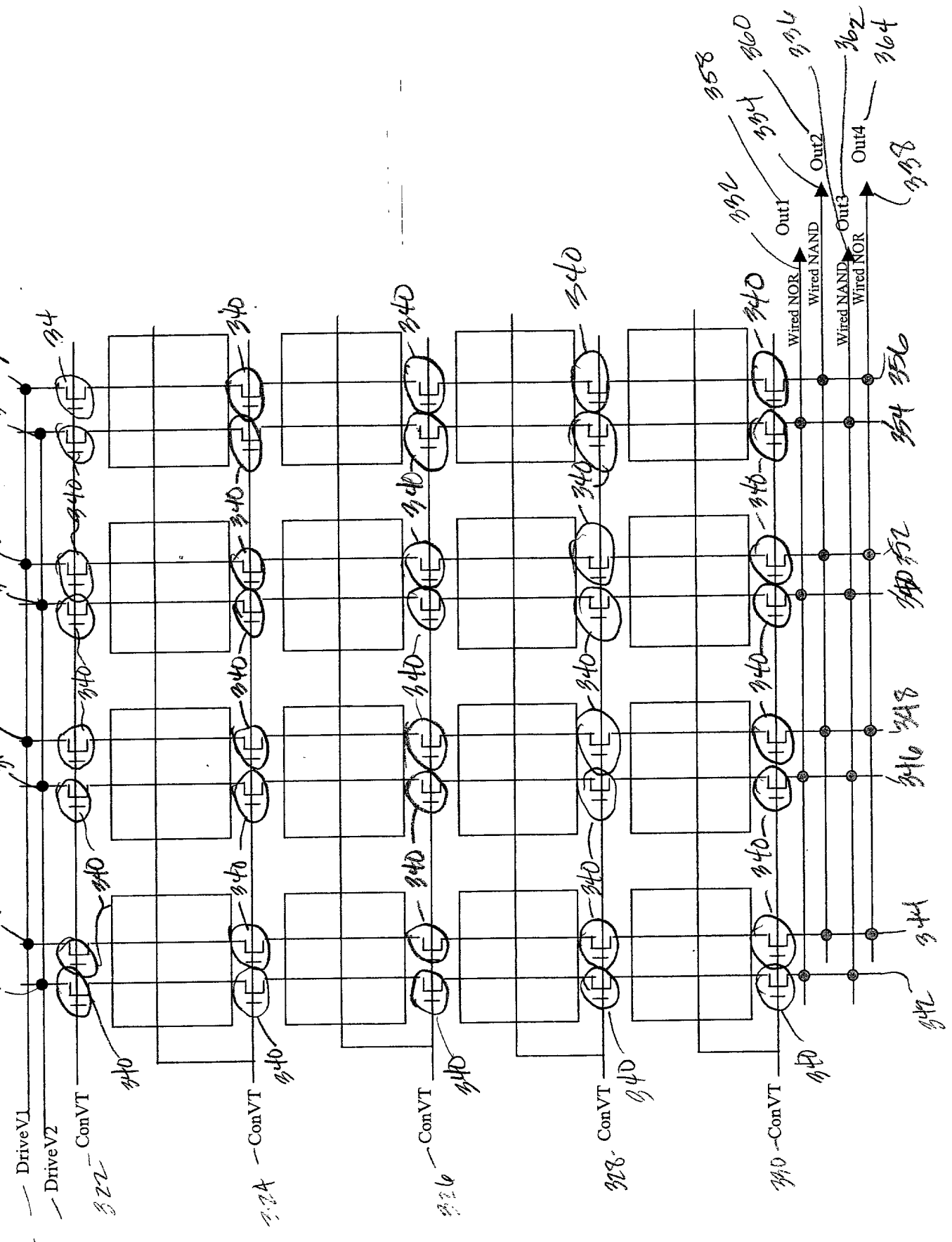

Vertical Track Testing Circuit
DriveV1
DriveV2
ConVT
Out1
Out2
Out3
Out4
Wired NOR
Wired NAND
Wired NAND
Wired NOR

FIG. 19

ACT-317

20050030080

Truth Table

DriveV1	DriveV2	Out1	Out2	Out3	Out4
0	0	1	1	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

Fig. 20

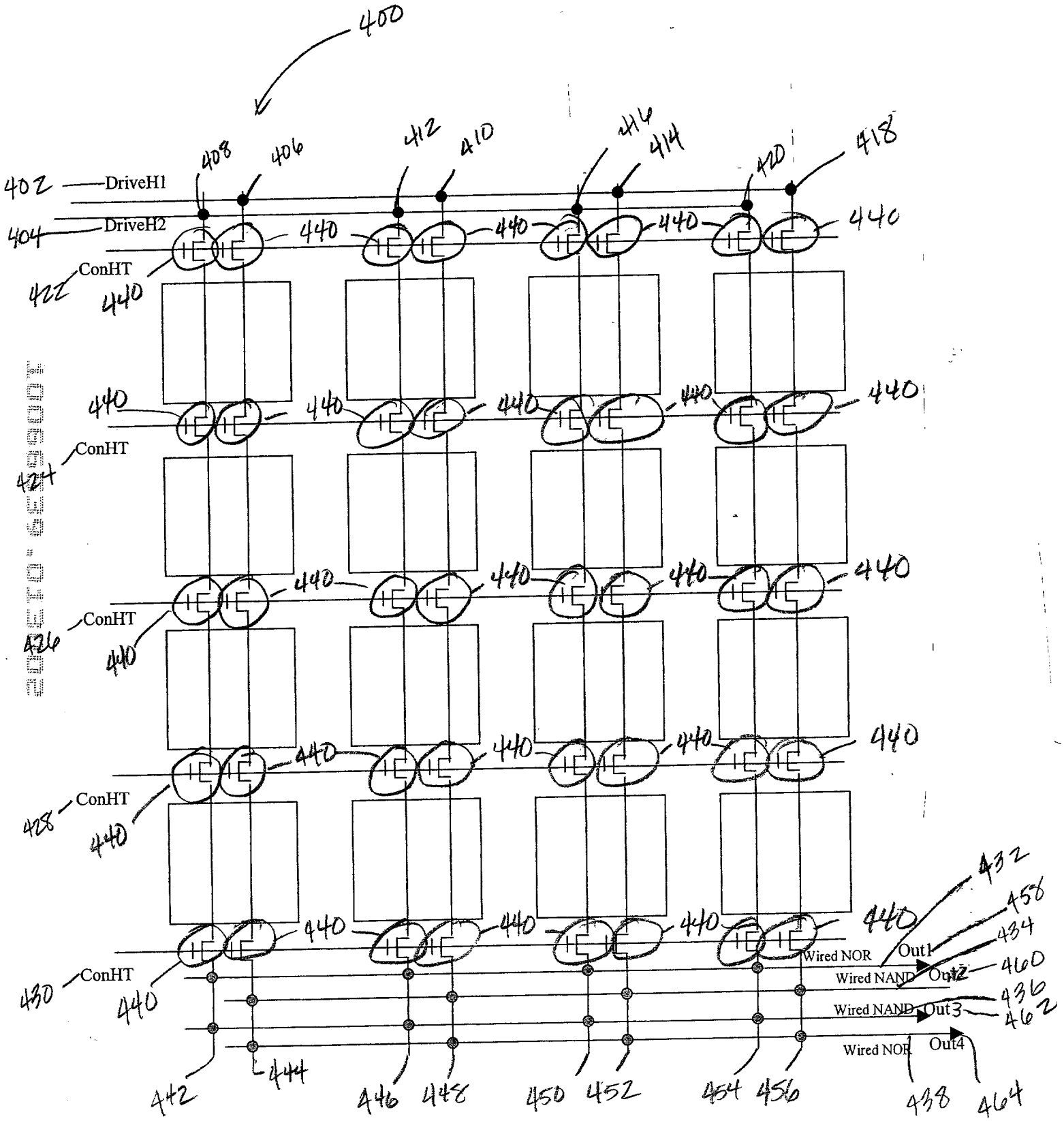

400
402
DriveH1
404
DriveH2
406
408
410
412
414
416
418
420
422
ConHT
424
ConHT
426
ConHT
428
ConHT
430
440
442
444
446
448
450
452
454
456
Wired NOR
Out1
Wired NAND
Out2
Wired NAND
Out3
Wired NOR
Out4
432
434
436
438
458
460
462
464

FIG. 21

ACT-317

20060538.0453602

Truth Table

DriveH1	DriveH2	Out1	Out2	Out3	Out4
0	0	1	1	1	1
0	1	1	0	1	0
1	0	0	1	0	1
1	1	0	0	0	0

FIG 22